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(54) Abstract Title
Low dielectric constant trench isolation structure

(57) The semiconductor device includes a substrate (110, 120) having an isolation trench 410 opening formed therein, a dielectric liner layer (310), such as silicon dioxide, formed within the isolation opening, and a low dielectric (K) material (410) formed over the dielectric layer and within the isolation opening to form an isolation structure for the semiconductor device. The low K material may be a spin on glass material, black diamond, silk, or other similar low K material.

FIG. 5

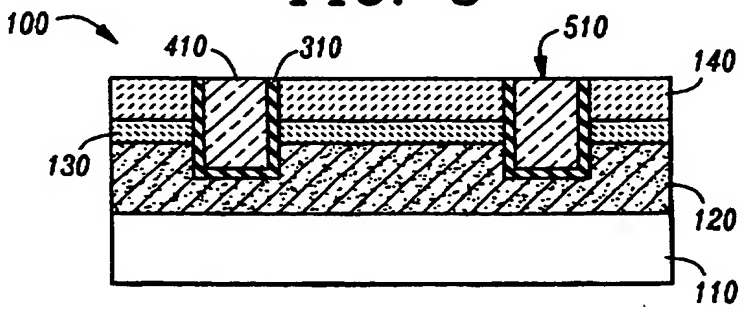

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FIG. 1

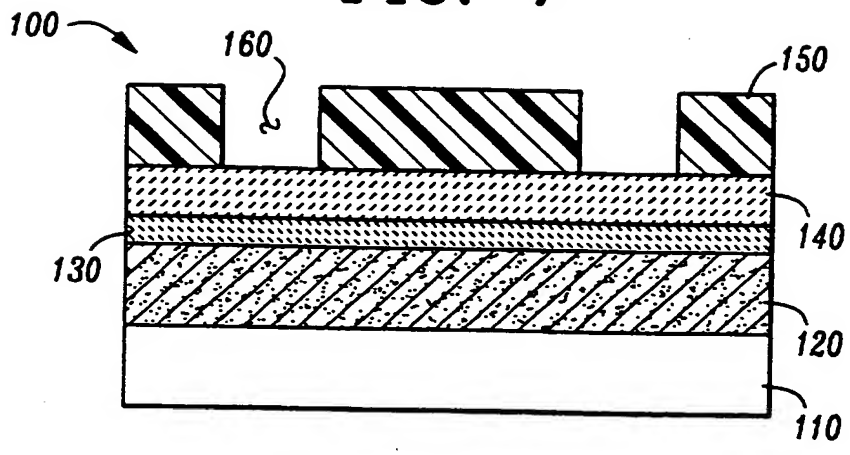


FIG. 2

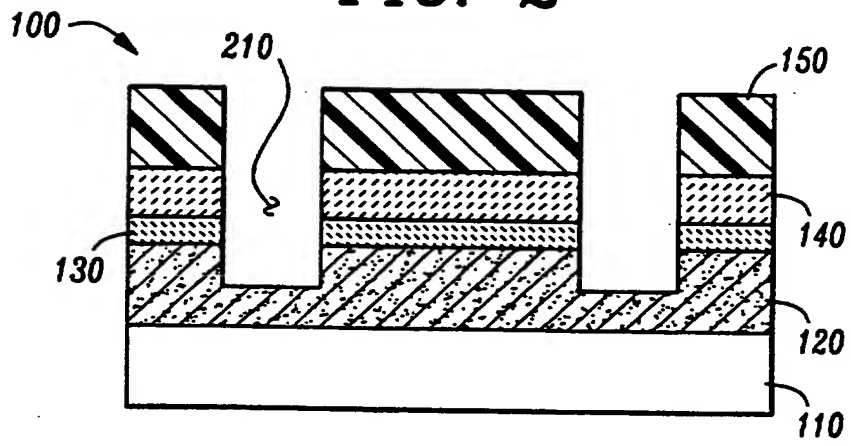


FIG. 3

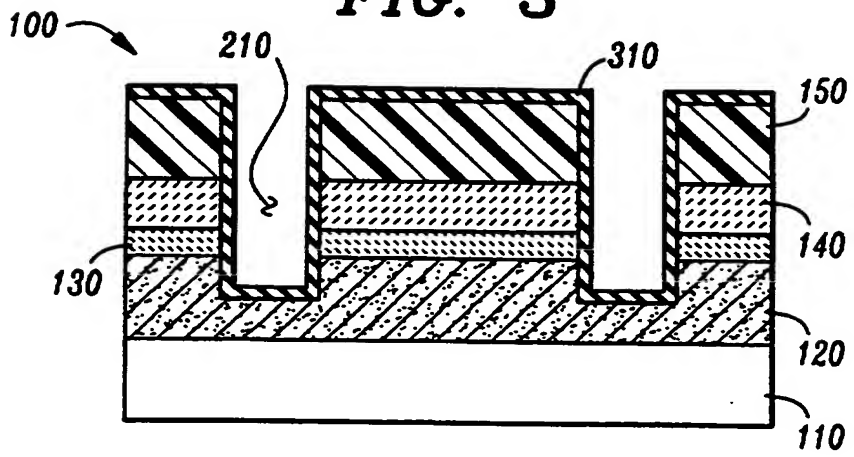


FIG. 4

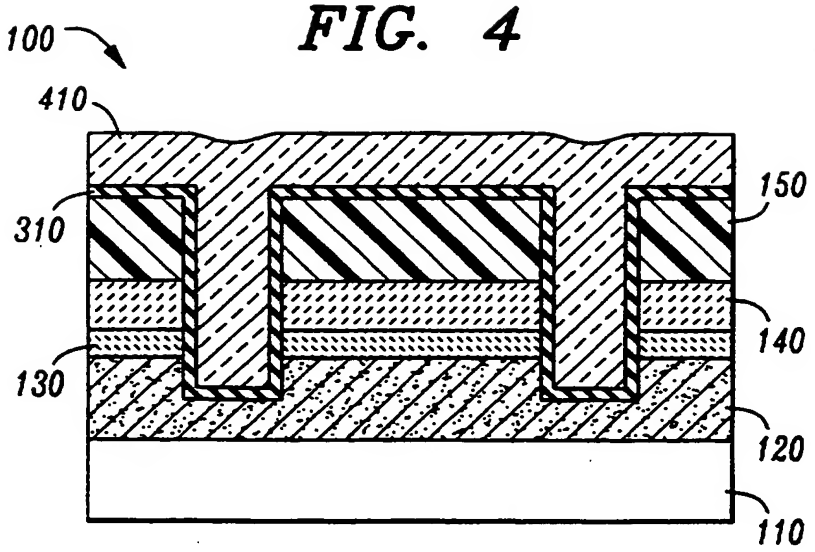


FIG. 5

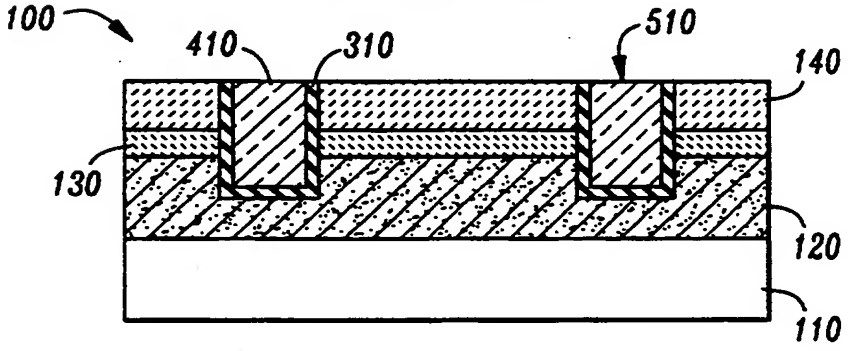
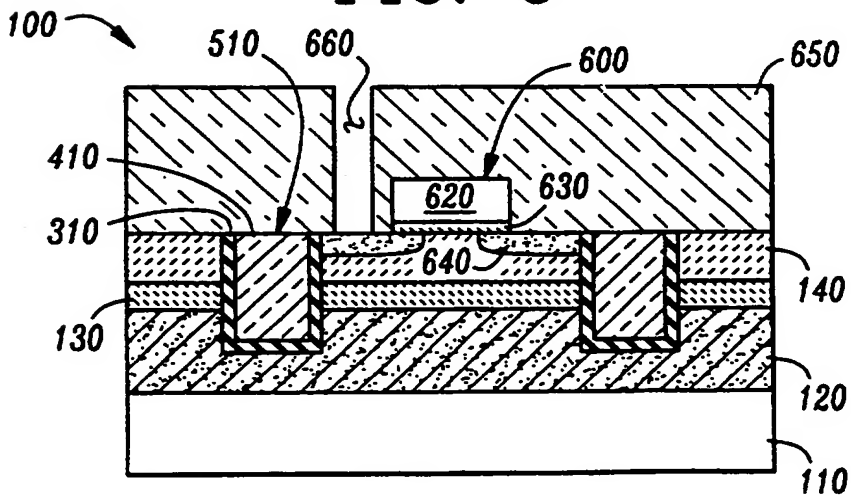


FIG. 6



SEMICONDUCTOR DEVICE HAVING A LOW K MATERIAL WITHIN A SHALLOW TRENCH ISOLATION AND A METHOD OF MANUFACTURE

Technical Field Of The Invention

The present invention is directed, in general, to a semiconductor device and, more specifically, to a semiconductor device having a low K material deposited within a shallow trench isolation structure and a method of manufacture thereof.

Background Of The Invention

Integrated circuits are now well known and extensively used in various technologies. Over the last decade, the operating speeds and packing densities have increased substantially while the device size has been dramatically reduced. The combination of increased packing density and device size reduction have posed ever new problems for the semiconductor fabrication industry that have not previously been a concern. One such area of fabrication involves the formation of isolation structures located on the same semiconductor wafer substrate, between transistor devices, to provide electrical isolation between the devices. A variety of techniques, generally termed isolation processes, have been developed to isolate such devices in integrated circuits.

One such process is local oxidation of silicon (LOCOS), in which a silicon nitride (Si_3N_4) film is used to isolate selected regions of the semiconductor substrate in which field oxide structures are formed. This isolation technique has been widely used as an isolation technique

of very large-scale integrated (VLSI) circuits. While this technique has been quite useful and extensively used in larger submicron devices, its use in smaller, present day submicron technologies has encountered geographical limitations due to the increased packing density.

To overcome the limitations associated with the LOCOS process, the industry devised an alternative isolation process known as shallow trench isolation (STI). This particular process provides an isolation structure that does require less surface area on the semiconductor substrate. However, even this process has encountered limitations in view of the increased packing density.

One such limitation concerns maintaining or increasing the threshold voltage while decreasing the capacitance. As well known, it is highly desirable to maintain a high threshold voltage of the isolation material associated with transistor devices, to minimize the formation of spurious conductive channels (i.e. current leakage) between transistor devices, which can cause device failure. In fact, it is even more desirable to increase the threshold voltage of such isolation structures, to insure that such leakage does not occur.

To maintain the desired levels of the isolation structure's threshold voltage, in view of the increased packing density, it is necessary to increase the structure's depth while maintaining present widths. Alternatively, one could maintain the present depth but increase the width. Both of these options are undesirable, however, for different reasons. Increasing the depth is undesirable because the resulting feature has

a high aspect ratio which can lead to voids within the structure. These voids are due to the difficulty of completely filling the structure with silicon dioxide. Increasing the width is equally undesirable, because the larger width occupies a greater amount of surface area and thus reduces the transistor packing density.

Capacitance is also a major concern in an isolation structure. It is highly desirable that the isolation structure have a low coupling capacitance so that the transistors' switching speeds are not adversely affected and parasitics are minimized. As discussed above, it is highly desirable to maintain or, even more preferably, increase the threshold voltage of the isolation structure in view of the increased performance demands and to minimize current leakage. However, increasing the threshold voltage, unfortunately, leads to a corresponding increase in capacitance. Thus, given the present state of the art, not only is it difficult to achieve the desired threshold voltage for the reasons stated above, but once the desired threshold voltage is achieved, it can cause an undesirable increase in the isolation structure's capacitance.

Accordingly, what is needed in the art is an isolation structure and a process for forming that isolation structure that avoids the disadvantages associated with prior art structures and processes.

Summary Of The Invention

To address the above-discussed deficiencies of the prior art, the present invention provides a semiconductor device having a unique isolation structure. In a

preferred embodiment, the semiconductor device includes a substrate having an isolation opening formed therein, a dielectric layer, such as silicon dioxide, formed within the isolation opening, and a low dielectric (K) material formed over the dielectric layer and within the isolation opening to form an isolation structure for the semiconductor device. In a preferred embodiment, the low K material has a dielectric constant less than a dielectric constant of the dielectric layer. The low K material may be a spin on glass material, black diamond, silk, or other similar low K materials.

Thus, the present invention, in a broad scope, provides for a unique isolation structure formed from a low K material that provides the desired level of threshold voltage at a low capacitance, with minimum leakage and parasitics.

The depth of the isolation opening may vary depending on design, process, and quality parameters. However, in one advantageous embodiment, the isolation opening has a depth of about 300 nm. The width may also vary but preferably has a width ranging from about 0.2 ☞m to about 0.4 ☞m. In another aspect of the present invention, the isolation structure has a threshold voltage of about 26 volts. However, the threshold voltage may also vary depending on design parameters. As briefly discussed above, capacitance is an important factor for isolation structures. In the isolation structure provided by the present invention, the capacitance is equally important. It is preferred that the capacitance be as low as possible, having as high a switching speed as possible. Thus, in one particular embodiment, the isolation

structure has a capacitance of about 4.87 nF/cm^2. This capacitance may be either higher or lower depending on design parameters.

The thickness of both the dielectric layer and the low K material may vary depending on the chosen depth of the isolation opening described above. However, in a preferred embodiment of the invention the thickness of the dielectric layer is about 20 nm and in another embodiment, the thickness of the low K material is about 280 nm.

In yet another aspect of the present invention, the semiconductor device further includes a transistor structure formed between a pair of the isolation structures. The transistor, which may be a CMOS device, may include conventional features such as a gate regions, and source/drain regions formed within a tub region. The unique isolation structures are formed on both sides of the transistor structure and provide electrical isolation between adjoining transistor structures. In one preferred embodiment, the isolation structure is formed in an epitaxial layer that has been conventionally formed on a semiconductor wafer.

The present invention, in another embodiment, provides for a method of manufacturing a semiconductor device having the above described isolation structure. In this particular aspect of the present invention, the method includes forming an isolation opening within a substrate of the semiconductor device, forming a dielectric layer within the isolation opening, and forming a low dielectric (K) material over the dielectric layer and within the isolation opening to form an isolation

structure for the semiconductor device.

The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

Brief Description Of The Drawings

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a sectional view of a semiconductor device covered by the present invention at an intermediate fabrication step;

FIGURE 2 illustrates a sectional view of the semiconductor device of FIGURE 1 following the formation of the isolation openings;

FIGURE 3 illustrates a sectional view of the semiconductor device of FIGURE 2 following the formation of a dielectric layer within the isolation openings;

FIGURE 4 illustrates a sectional view of the semiconductor device of FIGURE 3 following the formation of the low K dielectric material within the isolation openings;

FIGURE 5 illustrates a sectional view of the semiconductor device of FIGURE 4 following a planarization process; and

FIGURE 6 illustrates a sectional view of a transistor structure formed between the isolation structures.

Detailed Description

Referring initially to FIGURE 1 there is illustrated a sectional view of a semiconductor device 100 covered by the present invention at an intermediate fabrication step. Semiconductor device 100 is formed on a conventional semiconductor substrate 110. A conventionally formed epitaxial layer 120 is located on the semiconductor substrate 110. The epitaxial layer 120 may, of course, be doped with different dopants depending on the desired transistor design. While this particular embodiment includes the epitaxial layer 120, it should be understood that other embodiments may not include the epitaxial layer 120. A conventionally formed pad oxide layer 130 and nitride layer 140 are located over the epitaxial layer 120. The pad oxide layer 130 and nitride layer 140 serve as etching masks that improve the isolation process as described below. A photoresist layer 150 that has been conventionally formed and developed, is also shown. A portion of the photoresist layer 150 has been removed to form an etch guide openings 160 through which isolation openings will be later formed.

Turning now to FIGURE 2, there is illustrated a sectional view of the semiconductor device 100 shown in FIGURE 1 following the formation of isolation openings 210. The isolation openings 210 are formed by conventional etching techniques. As shown, the isolation openings 210 are formed into a tub region of the epitaxial layer 120. It should be noted, however, that because of the advantages associated with the present invention, the isolation openings' 210 size need not be increased to obtain higher threshold voltages as required in prior art isolation structures. In fact, the width of the isolation openings 210 may now be made even smaller without deepening them, thereby avoiding the problems associated with conventional isolation processes. Due to the advantages provided by the present invention, the threshold voltage can remain the same or even be increased, even though the isolation openings' 210 width may be made smaller. For example in one embodiment the width of the isolation openings 210 may range from about 0.2 ☞m to about 0.4 ☞m, and the depth may be about 300 nm.

FIGURE 3 illustrates a sectional view of the semiconductor device 100 as shown in FIGURE 2 following the formation of a dielectric layer 310 within the isolation openings 210. The dielectric layer 310 is preferably a silicon dioxide having a high dielectric constant of about 4.4. The dielectric layer 310 provides stress relief for the later deposited fill material, which in turn minimizes leakage.

Turning now to FIGURE 4, there is illustrated a sectional view of the semiconductor device 100 as shown in

FIGURE 3 following the formation of a low K dielectric material 410 within the isolation openings 210. For purposes of the present invention, low K is defined as any dielectric constant less that about 4.4. More preferably, however, the low K dielectric material 410 has a dielectric constant of about 2.1. The low K dielectric material 410 may be a spin on glass material. However, in an alternative embodiment black diamond, silk or other similar materials, which have a low K, may also be used. In one embodiment, the low K material has a thickness of 280 nm. The use of a low K material in the isolation openings 210 in place of the higher K materials, such as silicon dioxide, have shown unexpected and substantially improved results.

Turning briefly now to FIGURE 5, there is illustrated a sectional view of the semiconductor device 100 as shown in FIGURE 4 following a planarization process. Following the deposition of the low K material 410, the semiconductor device is planarized by a conventional chemical/mechanical process, which results in the completed isolation structures 510 as shown in FIGURE 5.

Following the planarization process, a transistor structure 600 is formed by a conventional process, resulting in the transistor structure 600 as shown in FIGURE 6. The transistor structure 600 is preferably, a metal oxide semiconductor (MOS) or, more preferably, a comparable metal oxide semiconductor (CMOS). In an exemplary embodiment, the transistor structure 600 includes a gate 620, formed on a gate oxide 630, which contact source and drain regions 640. The isolation structure 510, isolates the transistor structure 600 from

adjoining transistor structures that make up a MOS device. For example, where the MOS device is a CMOS device, the transistor structure 600 may be a p-type while the adjoining transistor structures would be n-type, thereby forming an npn CMOS device. Alternatively, however, the transistor structure 600 may be an n-type while the adjoining transistor structures would be p-type, thereby forming a pnp CMOS device. For further illustration, FIGURE 6 also illustrates a dielectric layer 650 having a contact opening 660 formed therein. Those who are skilled in the art understand how to complete the MOS device.

In one example as provided by the present invention, the isolation structure 510 was formed having a width of about 0.4 μm and a depth of about 300 nm. A 20 nm layer of silicon dioxide was conventionally deposited within isolation openings 210, followed by a deposition of a spin on glass material having a low K of about 2.1. Threshold voltage and capacitance tests were conducted on the present isolation structure 510 and on a conventional isolation structure having dimensions equal to the present isolation structure 510, the conventional isolation structure being filed with silicon dioxide, which is a high K dielectric material. The threshold voltage of the prior isolation structure was 15 volts while the isolation structure 510 provided by the present invention was about 26 volts, representing about a 76% improvement in the threshold voltage. Capacitance was also measured. The prior art isolation structure had a coupling capacitance of 8.63 nF/cm^2 while the isolation structure 510 provided by the present invention had a capacitance of about 4.87 nF/cm^2, representing about a 56% improvement in coupling capacitance. From the foregoing comparison, it is readily

apparent that the isolation structure 510 as provided by the present invention showed superior and unexpected results over prior art isolation structures.

Moreover, it is clear from the foregoing that the present invention provides a semiconductor device with a high threshold voltage, low coupling capacitance with minimum leakage and parasitics, without increasing the isolation structure's depth or width.

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

Claims:

1. A semiconductor device, comprising:

a substrate having an isolation opening formed therein;

a dielectric layer formed within the isolation opening; and

a low dielectric (K) material formed over the dielectric layer and within the isolation opening to form an isolation structure for the semiconductor device.

2. The semiconductor device as recited in Claim 1 wherein the low K material has a dielectric constant less than a dielectric constant of the dielectric layer.

3. The semiconductor device as recited in Claim 1 wherein the dielectric layer comprises silicon dioxide.

4. The semiconductor device as recited in Claim 1 wherein the low K material comprises a spin on glass material.

5. The semiconductor device as recited in Claim 1 wherein the low K material is black diamond or silk.

6. The semiconductor device as recited in Claim 1 wherein the isolation opening has a depth of about 300 nm.

7. The semiconductor device as recited in Claim 1 wherein the isolation opening has a width ranging from about 0.2 ☞m to about 0.4 ☞m.

8. The semiconductor device as recited in Claim 1 wherein the isolation structure has a threshold voltage of

about 26 volts.

9. The semiconductor device as recited in Claim 1 wherein the isolation structure has a capacitance of about 4.87 nF/cm^2.

10. The semiconductor device as recited in Claim 1 wherein a thickness of the dielectric layer is about 20 nm.

11. The semiconductor device as recited in Claim 1 wherein a thickness of the low K material is about 280 nm.

12. The semiconductor device as recited in Claim 1 further including a transistor structure formed between a pair of the isolation structures.

13. The semiconductor device as recited in Claim 12 wherein the transistor structure forms a transistor of a CMOS device.

14. The semiconductor device as recited in Claim 1 wherein the substrate is an epitaxial layer formed on a semiconductor wafer.

15. A method of manufacturing a semiconductor device, comprising:

forming an isolation opening within a substrate of the semiconductor device;

forming a dielectric layer within the isolation opening; and

forming a low dielectric (K) material over the dielectric layer and within the isolation opening to form

an isolation structure for the semiconductor device.

16. The method as recited in Claim 15 wherein forming the low K dielectric material includes forming a low K dielectric material having a dielectric constant less than the dielectric constant of the dielectric layer.

17. The method as recited in Claim 15 wherein forming the dielectric layer includes forming a silicon dioxide layer.

18. The method as recited in Claim 15 wherein forming the low K material includes forming a spin on glass material.

19. The method as recited in Claim 15 wherein forming the low K material includes forming black diamond or silk.

20. The method as recited in Claim 15 wherein forming an isolation opening includes forming the isolation opening to a depth of about 300 nm.

21. The method as recited in Claim 15 wherein forming the isolation opening includes forming the isolation opening to a width ranging from about 0.2 ☞m to about 0.4 ☞m.

22. The method as recited in Claim 15 wherein forming an isolation structure includes forming the isolation structure having a threshold voltage of about 26 volts.

23. The method as recited in Claim 15 wherein forming an isolation structure includes forming the isolation structure having a capacitance of about 4.87 nF/cm^2.

24. The method as recited in Claim 15 wherein forming a dielectric layer includes forming a dielectric layer to a thickness of about 20 nm.

25. The method as recited in Claim 15 wherein forming a low dielectric material includes forming a low dielectric material to a thickness of about 280 nm.

26. The method as recited in Claim 15 further including forming a transistor structure between a pair of the isolation structures.

27. The method as recited in Claim 26 wherein forming the transistor structure forms a transistor of a CMOS device.

28. The method as recited in Claim 15 wherein forming a substrate includes forming an epitaxial layer on the semiconductor wafer.

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Application No: GB 0030010.3
Claims searched: 1-28

Examiner: Steven Morgan
Date of search: 27 September 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H1K(KGCCT)

Int Cl (Ed.7): H01L 21/762

Other: Online: WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0 678 912 A2	(TEXAS INSTRUMENTS) See whole document.	1-28
X	EP 0 553 904 A1	(IBM) See whole document.	1-3, 5-13, 15-17, & 19-27
X	US 5 702 976	(MICRON) See whole document.	1-28

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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